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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,969	09/22/2003	Katsumi Abe	q75817	4962

23373 7590 11/23/2009

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EXAMINER	
PHAM, TAMMY T	
ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
11/23/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/664,969	ABE, KATSUMI	
	Examiner	Art Unit	
	TAMMY PHAM	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26 and 29-36* is/are pending in the application.

4a) Of the above claim(s) *8-15 and 22-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,16-21 and 29-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 9/23/09.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Claims 27-28 have been cancelled. Claims 8-15, 22-26 have been withdrawn. Claims 1-7, 16-21, 29-36 are considered below.

Response to Arguments

2. Applicant's arguments filed 31 August 2009 have been fully considered but they are not persuasive.

§ 112 Rejection

3. **In regards to claims 4, 19,** Applicant's amendments filed 31 August 2009 overcome the prior rejection hence the prior 112, 2nd rejection has been withdrawn.

§ 103 Rejection

4. **In regards to independent claim 1,** Applicant submits that the prior art of record fails to read upon the newly amended claim language. In particular, that *"Yanagi does not teach or suggest a signal line connected to each gate terminal of the first and second transistors, which control the switching of the first and second transistors (Remarks 21-22)."* This is not persuasive.

5. First of all, there is no explicit support for the new limitation. Further, the claim language remains broad enough that Yanagi continues to read upon the amendments. In particular, the newly amended claim language simply recites that the new signal line controls the

switching of the transistors. Yanagi teaches that the transistors are turned off and on by the signal line (column 11, lines 20-40), hence Yanagi continues to read upon the claim language as currently stated.

6. **In regards to independent claim 1,** Applicant submits that it would not have been obvious to combine Yanagi and Okajima because *"replacing a constant DC voltage at Vref1 with the output of the clock-pulse arrangement determination unit would change the primary function of the offset setting section of Yanagi (Remarks 22)."* This is not persuasive.

7. The constant DC voltage is not being replaced with the output of the clock-pulse. The structure of Yanagi is the main reference, and what is being combined is the concept of Okajima that have the transistors set up as claimed. It would have been obvious to incorporate the switching device of Okajima with the transistors arranged as such, with the switching device of Yanagi. The benefit of this combination is that this switching configuration would allow for higher speed and frequency (Okajima).

8. Replacing the switch of Yanagi with the transistors of Okajima will not change the primary function of Yanagi. The primary objective of Yanagi is to "provide an active matrix type display device which can clear an imbalance of an effective voltage even though refresh periods of a different length exist in a mixed manner (column 3, lines 25-30)." There is no explicit or implicit teachings in Yanagi that require that the switch of the device must not be changed. As such, one skilled in the art would realized that a switch can take a variety of different forms, one form is of a transistor. It is well known in the art that a transistor may operate as a switch. Hence, it would have been obvious to one with ordinary skill in the art at the

time the invention was made to replacing the switch of Yanagi with the transistors of Okajima. This combination would not destroy the primary function of Yanagi, since there is no teaching on Yanagi which prohibits the use of transistors from being used as a switch, and it is common in the art to incorporate the use of transistors as a switch.

9. **In regards to independent claim 1,** Applicant submits that *"Applicant's specification does provide at least one advantage for the claimed feature... [hence] the voltage values of the signal lines are not an obvious matter of design choice (Remarks 22-23)."* This is not persuasive.

10. First of all, the cited portion teaches the claimed limitations but does not provide an explicit advantage as Applicant alleges. Second, even assuming that there is support for the claim limitation, that is equally strong support for having the voltage values be *"substantially same"* hence, it would appear that it would be obvious to interchange the two concept, of whether the voltage values are substantially the same or higher/lower than one another, since the device would work equally as well.

11. Further, the advantages Applicant has cited are not unexpected advantages, and whether the voltages are different -as claimed- or are the same, the end result overall would be equally as efficient in achieving the predictable result of supplying the adequate value to the common electrode. Please also refer to MPEP 2145, subsection II.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

12. Claims 1-7, 16-21, 29-36 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

13. **In regards to independent claims 1, 17, 33, 34,** the newly amended claim language teaches of at least one signal that *"which controls the switching of the first and second transistors (line 10)."* However, there is no explicit support for this limitation. Appropriate correction is necessary.

14. **In regards to claims 2-7, 16, 18-21, 29-32, 35-36,** these claims are being rejected for being dependent upon improperly worded independent claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 1, 3, 16-19, 21, 29, 31-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagi et al. (U.S. Patent No.: 7,002,541 B2) in view of Okajima (U.S. Patent No.: 5,793,680).

16. **In regards to independent claims 1, 33-34,** Yanagi teaches of a common drive circuit (Fig. 1, items 4-6) for a display (Fig. 1, item 12), the common drive circuit (Fig. 1, items 4-6) comprising:

17. a first voltage supply (Fig. 1, item Vcom2) and a second voltage supply (Fig. 1, item Vcom1) which respectively supply a high level voltage signal (Fig. 2, item Vcom2) and a low level voltage signal (Fig. 2, item Vcom1) to a common electrode (Fig. 1, item Vcom);

18. at least one signal line (Fig. 1, item Vref); and

19. at least one capacitance load (Fig. 1, item 13) connected to respective terminals of the switch (Fig. 1, item 5c) not connected to the first and second voltage supplies (Fig. 1, items Vcom1, Vcom2),

20. wherein a high level of a signal passing through the at least one signal line (Fig. 1, item Vref1) is substantially equal to the high level voltage signal supplied by the first voltage supply (Fig. 1, item Vcom2) and a low level of the signal passing through the signal line (Fig. 1, item

Vref2) is substantially equal than the low level voltage signal supplied by the second voltage supply (Fig. 1, item Vcom1).

21. Yanagi fails to teach of at least one first transistor including either a drain or a source terminal connected to the first supply;

22. at least one second transistor including either a drain or source terminal connected to the second supply;

23. at least one signal line connected to each gate terminal of the first and second transistors; which controls the switching of the first and second transistors; and

24. at least one load connected to respective terminals of the first and the second transistors,

25. wherein a high level of a signal passing through the at least one signal line is higher than the high level voltage signal supplied by the first voltage supply and a low level of the signal passing through the signal line is lower than the low level voltage signal supplied by the second voltage supply.

26. Applicant has not disclosed any specific advantage or criticality to having a high level of a signal passing through the at least one signal line is higher than the high level voltage signal supplied by the first voltage supply and a low level of the signal passing through the signal line is lower than the low level voltage signal supplied by the second voltage supply. As such, the high and low values are an obvious matter of design choice.

27. It would have been obvious to one with ordinary skill in the art at the time the invention was made to have the high (or low) level of the signal line be either substantially equal to the first and second voltage supply as taught by Yanagi or greater and lower than the first and second voltage supplies as claimed, since either of the values would be sufficient in achieving the predictable result of supplying the adequate value to the common electrode. And further, even Applicant teaches that either value may be supplemented for the other (sections [0019, 0069]).

28. Okajima teaches of at least one first transistor (Fig. 14, items 62, 66) including either a drain or a source terminal connected to the first supply (Fig. 14, item 15B);

29. at least one second transistor (Fig. 14, item 65, 69) including either a drain or source terminal connected to the second supply (Fig. 14, item 15B);

30. at least one signal line (Fig. 14, item L1) connected to each gate terminal of the first and second transistors (Fig. 14, items 62, 66 and 65 and 69) which controls the switching of the first and second transistors (Fig. 14, items 62, 66 and 65 and 69); and

31. at least one load (Fig. 14, item /CLKO) connected to respective terminals of the first and the second transistors (Fig. 14, items 62, 66 and 65, 69).

32. It would have been obvious to one with ordinary skill in the art at the time the invention was made to replace the switch of Yanagi with the first and second transistors as taught by Okajima. This combination would allow for a circuit with high speed signal frequency (Okajima, column 1, lines 8-10).

33. **In regards to independent claim 17,** in addition to the claim limitations of claim 1 above, Yanagi further teaches of a display (Fig. 1) comprising:

34. a substrate (Fig. 1):

35. a display portion (Fig. 1, item 13) integrated on the substrate; and

36. a gate driver circuit (Fig. 1, item 2) which controls switching of pixels (Fig. 1, item 13) of each line in a display portion (Fig. 1, item 13);

37. a common drive circuit (Fig. 1, items 4-6) for the display portion (Fig. 1, item 13) which simultaneously driving capacitance loads in the display portion (Fig. 1, item 13).

38. **In regards to claim 16,** Yanagi teaches that at least the common drive circuit (Fig. 1, items 4-6), a display portion (Fig. 1, item 13) and a gate driver circuit (Fig. 1, item 2) for controlling switching of pixels of each line in the display portion (Fig. 1, item 13) are mounted on a substrate, and

39. wherein the common drive circuit (Fig. 1, items 4-5, Vcom) is disposed on a position opposite to the gate driver circuit (Fig. 1, item 2) and the display portion therebetween (Fig. 1, item 13).

40. **In regards to claims 3, 18,** Okajima teaches that at least one first transistor (Fig. 14, items 62, 66) comprises P-type transistor (Fig. 14, item 62) and the at least one second transistors (Fig. 14, items 65, 69) comprises N-type transistor (Fig. 14, item 69), and

41. wherein the gate terminals of the first (Fig. 14, items 62, 66) and second transistors (Fig. 14, item 62) are connected to common signal lines (Fig. 14, item /CLKO).

42. **In regards to claim 19,** Okajima teaches that the P-type transistors (Fig. 14, item 62) and N-type transistors (Fig. 14, item 66) are connected in parallel to be the first transistor (Fig. 14, items 62, 66), and N-type transistors (Fig. 14, item 69) and P-type transistors (Fig. 14, item 65) are connected in parallel to be the second transistor (Fig. 14, item 65, 69),

43. wherein respective gates of the P-type transistors of the first transistor (Fig. 14, item 62) and the N-type transistor of the second transistors (Fig. 14, item 69) are connected to one the signal line (Fig. 14, item L1), and respective gates of the N-type transistors of the first transistor (Fig. 14, item 66) and the P-type transistors of the second transistor (Fig. 14, item 65) are connected to an inversion signal line of one the signal line (Fig. 14, item L2).

44. **In regards to claim 21,** Yanagi as modified by Okajima fails to teaches that the first and second transistors are comprised of thin-film transistors.

45. Examiner takes official notice that it is well known in the art to use thin-film transistors.

46. It would have been obvious to one with ordinary skill in the art at the time the invention was made to use thin-film transistors in the drive circuit of Yanagi as modified by Okajima, since the use of thin-film transistors enables a simple and cost efficient method to implement a switching method.

47. **In regards to claims 29, 31-32,** Yanagi as modified by Okajima teaches of a level shift circuit (Yanagi , Fig. 1, items 5a-b or Okajima, Fig. 14, item 60) connected to the one signal line directly (Yanagi , Fig. 1, item Vref1) {claim 29}; and

48. the inversion signal line directly (Okajima, Fig. 14, item 56) {claims 30-32}.

49. **In regards to claim 35,** Yanagi as modified by Okajima teaches that the at least one capacitance (Yanagi, Fig. 1, item 13) is directly connected to respective terminals of the first and second transistors (Okajima, Fig. 14, item 62, 66 and 65, 69).

50. **In regards to claim 36,** Yanagi teaches that of a common voltage generating circuit (Fig. 1, items 4-6) formed on the substrate adjacent to the common drive circuit (Fig. 1, items 4-6).

51. Claims 5, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagi et al. (U.S. Patent No.: 7,002,541 B2) in view of Okajima (U.S. Patent No.: 5,793,680) and Park et al. (U.S. Patent No.: 7,133,034 B2).

52. **In regards to claims 5, 20,** Yanagi and Okajima fails to teach that a high level voltage of each signal of the signal line is a high-level line voltage of the gate driver and

53. wherein a low-level voltage of each signal of the signal line is a low-level line voltage of the gate driver (Fig. 1).

54. Park teaches that a high level voltage of each signal of the signal line is a high-level line voltage of the gate driver and

55. wherein a low-level voltage of each signal of the signal line is a low-level line voltage of the gate driver (Fig. 1).

56. It would have been obvious to one with ordinary skill in the art at the time the invention was made to have the high and low signal of the signal line is the high and low signal of the gate line as taught by Park with the display of Yanagi and the transistors of Okajima. This combination would allow for the gate to open so that the common voltage may be applied (Park, Fig. 1).

57. Claims 2, 4, 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagi et al. (U.S. Patent No.: 7,002,541 B2) in view of Okajima (U.S. Patent No.: 5,793,680) and Kubota et al. (U.S. Publication No.: 2002/0075249 A1).

58. **In regards to claim 2,** Yanagi teaches that at least the common drive circuit (Fig. 1, items 4-6), a display portion (Fig. 1, item 13) and a gate driver circuit (Fig. 1, item 2) for controlling switching of pixels of each line in the display portion (Fig. 1, item 13) are mounted on a substrate, and

59. wherein the common drive circuit (Fig. 1, items 4-5, Vcom) is disposed on a position opposite to the gate driver circuit (Fig. 1, item 2) and the display portion therebetween (Fig. 1, item 13).

60. Yanagi fails to teach that display and driver are placed on a single substrate.

61. Kubota teaches that display and driver are placed on a single substrate (Fig. 76, section [0303]).

62. It would have been obvious to one with ordinary skill in the art at the time the invention was made to have all the elements of Yanagi be combined on a single substrate as taught by Kubota. This combination can reduce cost and improve reliability (Kubota, section [0303]).

63. **In regards to claim 4,** Okajima teaches that the P-type transistors (Fig. 14, item 62) and N-type transistors (Fig. 14, item 66) are connected in parallel to be the first transistor (Fig. 14, items 62, 66), and N-type transistors (Fig. 14, item 69) and P-type transistors (Fig. 14, item 65) are connected in parallel to be the second transistor (Fig. 14, item 65, 69),

64. wherein respective gates of the P-type transistors of the first transistor (Fig. 14, item 62) and the N-type transistor of the second transistors (Fig. 14, item 69) are connected to one the signal line (Fig. 14, item L1), and respective gates of the N-type transistors of the first transistor (Fig. 14, item 66) and the P-type transistors of the second transistor (Fig. 14, item 65) are connected to an inversion signal line of one the signal line (Fig. 14, item L2).

65. **In regards to claim 6,** Yanagi as modified by Okajima fails to teaches that the first and second transistors are comprised of thin-film transistors.

66. Examiner takes official notice that it is well known in the art to use thin-film transistors.

67. It would have been obvious to one with ordinary skill in the art at the time the invention was made to use thin-film transistors in the drive circuit of Yanagi as modified by Okajima, since the use of thin-film transistors enables a simple and cost efficient method to implement a switching method.

68. **In regards to claim 7,** Yanagi teaches that the display portion comprises a liquid crystal display (Fig. 1).

69. **In regards to claim 30,** Yanagi as modified by Okajima teaches of a level shift circuit (Yanagi , Fig. 1, items 5a-b or Okajima, Fig. 14, item 60) connected to the one signal line directly (Yanagi , Fig. 1, item Vref1) {claim 29}; and

70. the inversion signal line directly (Okajima, Fig. 14, item 56) {claims 30-32}.

Conclusion

71. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

72. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

73. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammy Pham whose telephone number is (571) 272-7773. The examiner can normally be reached on 8:00-5:30 (Mon-Fri).

74. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

75. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TP
16 November 2009

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/Tammy Pham/
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